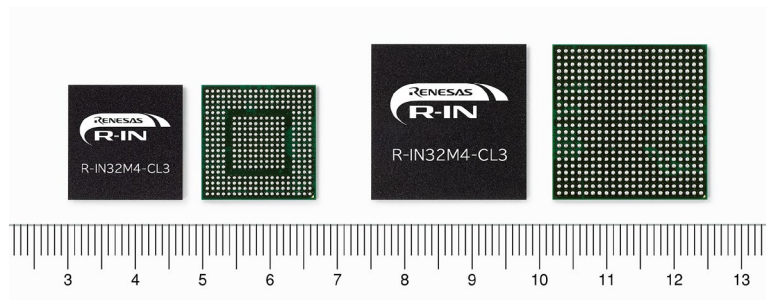


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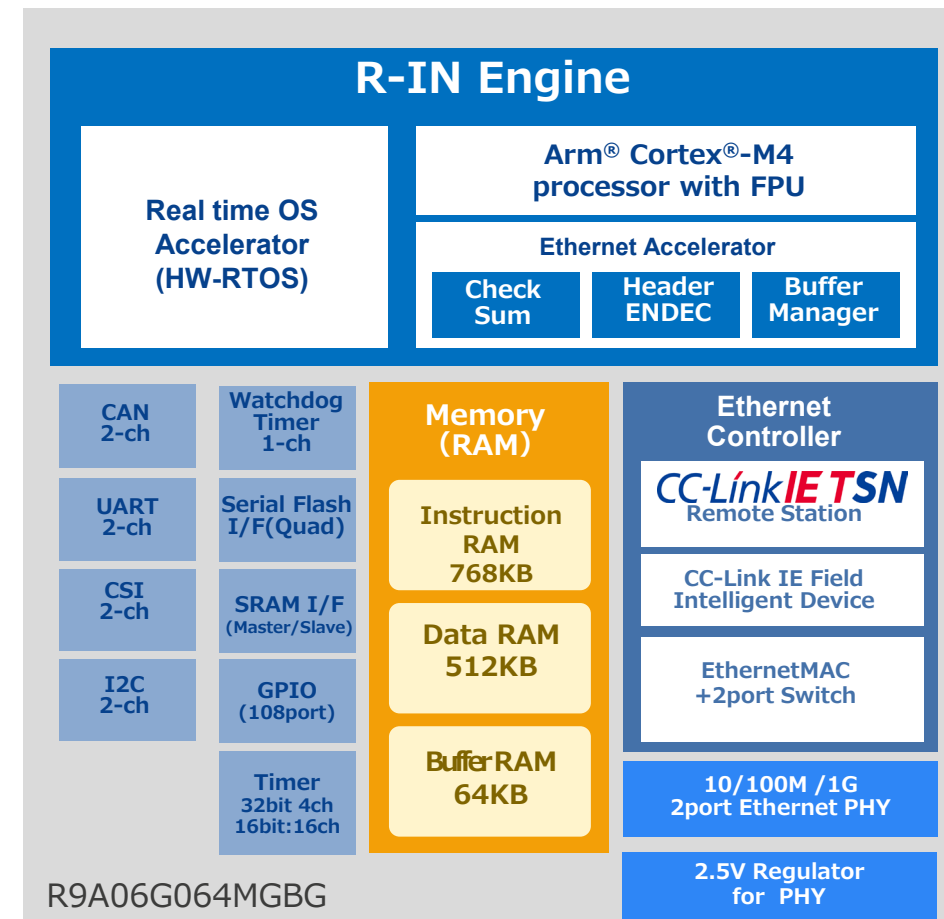
R-IN32M4-CL3

R9A06G064MGBG/R9A06G064SGBG

- Time synchronization accuracy less than $\pm 1\mu\text{s}$ between devices.
- 2-port GbE-enabled PHY, CPU, and RAM (1.3MB) on a single chip
- multi-protocol support with R-IN engine
- Small package and built-in regulator for PHY reduce footprint of PCB .
- **Low Power consumption** (35 % reduction vs. R-IN32M4-C2)



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TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan

URL: <https://www.renesas.com/>

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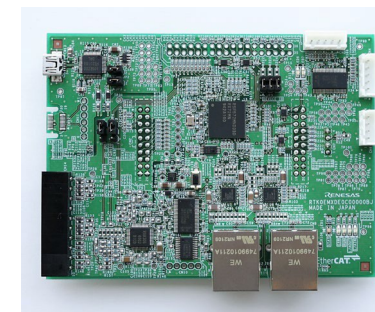
RX72M Industrial Network Solution

CC-Link IE TSN Class A Solution

- Easy to evaluate for CC-Link IE TSN Class A with Renesas RX72M CPU card ([RTK0EMXDE0C0000BJ](#)) and partner board ([TS-RX72M-COM](#))
- Sample code (Evaluation purpose) and Application note are available free of charge from Renesas website, suitable for initial evaluation [RX72M Network Solution](#)
- Protocol stack for mass production are supported by our partner (Sherpa Inc.), enables to realize CC-Link IE TSN Class A only by software implementation



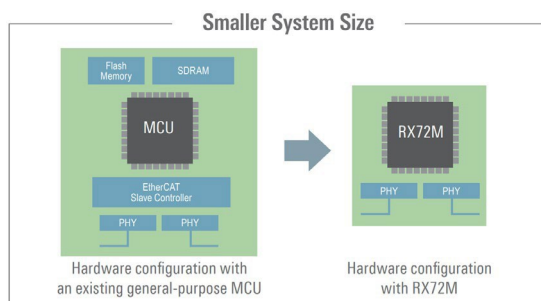
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RX72M CPU card

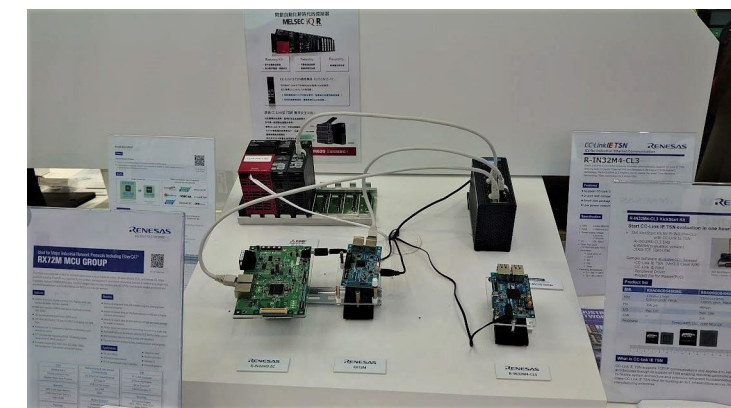


TS-RX72M-COM



RX72M 240MHz 32-Bit RXv3 core / 8Kbyte cache			
Memory <ul style="list-style-type: none"> 80M (Flash) + 512M (RAM) (Cache) 1MB Dual Bank + 32KB (for ECC) -32KB (Stack) 8KB (Standby) Background Operation 	Timer <ul style="list-style-type: none"> PWM TIMERS <ul style="list-style-type: none"> 10k x 8ch, 32bit x 1ch (MTU) 10k x 1ch (TPC) 32k x 4ch (GPTA) General Timers <ul style="list-style-type: none"> 10k x 1ch (TMR) 32k x 4ch (CMPT) 32k x 1ch (CMT) 32k x 1ch (CMT) Real-time clock (RTC) 	Connectivity <ul style="list-style-type: none"> Ethernet 10/100 base x 2ch 1st EtherCAT slave controller 100BASE-TX Full Speed 11P x 1ch COM x 3ch 40 Base x 1ch, MMC Bus x 1ch Serial Communication <ul style="list-style-type: none"> UART x 1ch (w/ Single SPI / IC) SPI x 3ch DC x 3ch 	Security & Encryption <ul style="list-style-type: none"> Cryptography <ul style="list-style-type: none"> AES/TDES/SERIAL/SAS/SHA TSEC Key management Access management Memory protect Secure ID
External Memory <ul style="list-style-type: none"> 18V/20kV external bus (SDRAM, SDRAM) Quad SPI x 1ch 	System, Power Management <ul style="list-style-type: none"> EMAC x 8ch, DTC 2.5V/3.3V x 2ch Internal open-drain High-speed on-chip oscillator Event Link controller 	Analog <ul style="list-style-type: none"> 12bit ADC x 2ch 2 independent can 3ch on-chip analog S/H (Fast) 12bit DAC x 2ch Temperature sensor A-2 Insulator BF x 6ch 	Human-Machine Interface (HMI) <ul style="list-style-type: none"> CMOS camera I/F Graphics - LCD US x 2ch
	Safety Functions <ul style="list-style-type: none"> Watchdog timer x 2ch ADC calculator PWM wave output shutdown Future Object extend (Clock, Memory, Analog) 	Accelerator <ul style="list-style-type: none"> High-resolution function 3D drawing engine 	

The maximum specifications for the group are shown



Solution example for RX72M, R-IN32M4-CL3 Exhibited at Automation Taipei (2023)

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